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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/846,801	TALAGALA, NISHA D.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-20,22-34 and 36-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,8,23,24,37 and 38* is/are allowed.

6)☒ Claim(s) *1-4,6,9-12,14-20,22,25-28,30-34,36,39-42 and 44* is/are rejected.

7)☒ Claim(s) *13,29 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-4, 6, 15-20, 22, 31-34, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6442711 to Sasamoto et al. Referring to claims 1 and 31, Sasamoto et al. disclose detecting data integrity errors in the storage device; counting each data integrity error in a count (From line 43 of column 4, "If a disk drive reports that it overcame some errors by itself in the course of the Read/Write operation, the MPU 104 counts up the number of errors of the disk drive and calculates some other values, such as "total access size", "total number of errors" and "total access size when an error is detected", and stores them in the table."); when the count reaches a threshold limit, placing the storage device into a forced failure state (From line 36 of column 5, "The calculating means 302 calculates an error rate and its inclination value from the total number of errors and the total access size of the disk drive in a way described later in FIG. 6 (see step S10). The judging means 303 judges if the disk drive is in need of disk changes from the total number of errors, the error rate, and the error rate inclination. When none of the calculated values exceeds the threshold value specified in the system, the disk array control unit 101 waits for further Read/Write requests from the host computer 100. If at least one of the calculated values exceeds the threshold value (however there may be some other combinations of the them, see step S11). The executing means 304

regards the disk drive as half-failed (see step 12). The reproducing means 307 copies or regenerates the data on the half-failed disk drive (see step S13), and stores the reproduced data on the spare disk drive 103c (see step S14). Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18). Then the disk array control unit 101 waits for further Read/Write requests from the host computer 100."); returning the storage device from the forced failure state to an operational state (From line 51 of column 5, "Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18)."); and setting the count to a base level (From the abstract, "The control unit includes means for storing a history of self recovered errors of each one of the plurality of data storage devices, means for calculating an error rate of each of the plurality of data storage devices on the basis of the history of errors, means for judging a necessity to execute a preventive maintenance of each one of the plurality of data storage devices from the error rate, and means for executing the preventive maintenance.")..

Referring to claims 2, 16, and 32, Sasamoto et al. disclose the storage device is a hard disk drive (From figure 1, element 103.).

Referring to claims 3 and 33, Sasamoto et al. disclose reconstructing data stored on the storage device in a restoration storage device (From line 48 of column 5, "The reproducing means 307 copies or regenerates the data on the half-failed disk drive (see step S13), and stores the reproduced data on the spare disk drive 103c (see step S14).").

Referring to claims 4 and 34, Sasamoto et al. disclose providing a storage device array containing said restoration storage device and said storage device (See figure 3.).

Referring to claims 6 and 36, Sasamoto et al. disclose said returning the storage device from the forced failure state to an operational state comprises reformatting the storage device (From line 51 of column 5, "Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18).").

Referring to claims 13, 29, and 43, Sasamoto et al. disclose tracking the time elapsed after a first data integrity error; and decreasing the count if the time elapsed after the first data integrity error and before a second data integrity error is greater than a preset refresh period (From line 61 of column 5, "FIGS. 6(a), 6(b), and 6(c) are diagrams illustrating how to calculate the error rate and its

inclination shown in step S10 of FIG. 5. In each of FIGS. 6(a), 6(b), and 6(c), the vertical axis shows the total number of errors and the horizontal axis shows the total access size. In FIG. 6(a), a total number of errors is marked with a dot against a total access size when an error is detected. A line segment is drawn as an approximate line segment of the dots in each predetermined interval. The line segment shows a normal transition at the beginning and then exceeds the threshold level in the middle of the second interval. Subsequently, the judging means 303 judges that the disk drive needs to be exchanged. If the judging means 303 judges the necessity of preventive maintenance from an error rate and its inclination in addition to the total number of errors, the threshold level can be set up with a more appropriate value which is higher than a conventional level.").

Referring to claim 15, Sasamoto et al. disclose a storage system, comprising: a storage device; and a demerit monitor coupled to the storage device operable to detect data integrity errors in the storage device, count each data integrity error in a count (From line 43 of column 4, "If a disk drive reports that it overcame some errors by itself in the course of the Read/Write operation, the MPU 104 counts up the number of errors of the disk drive and calculates some other values, such as "total access size", "total number of errors" and "total access size when an error is detected", and stores them in the table."), when the count reaches a threshold limit, place the storage device into a forced failure state (From line 36 of column 5, "The calculating means 302 calculates an error rate and its inclination value from the total number of errors and the total access

size of the disk drive in a way described later in FIG. 6 (see step S10). The judging means 303 judges if the disk drive is in need of disk changes from the total number of errors, the error rate, and the error rate inclination. When none of the calculated values exceeds the threshold value specified in the system, the disk array control unit 101 waits for further Read/Write requests from the host computer 100. If at least one of the calculated values exceeds the threshold value (however there may be some other combinations of the them, see step S11). The executing means 304 regards the disk drive as half-failed (see step 12). The reproducing means 307 copies or regenerates the data on the half-failed disk drive (see step S13), and stores the reproduced data on the spare disk drive 103c (see step S14). Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18). Then the disk array control unit 101 waits for further Read/Write requests from the host computer 100."); return the storage device from the forced failure state to an operational state (From line 51 of column 5, "Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see

step S18).”); and set the count to a base level (From the abstract, “The control unit includes means for storing a history of self recovered errors of each one of the plurality of data storage devices, means for calculating an error rate of each of the plurality of data storage devices on the basis of the history of errors, means for judging a necessity to execute a preventive maintenance of each one of the plurality of data storage devices from the error rate, and means for executing the preventive maintenance.”)..

Referring to claim 17, Sasamoto et al. disclose a hard disk controller, wherein said hard disk controller includes said demerit monitor (From line 24 of column 3, “The disk array control unit 101 includes a MPU 104, a RAM 105, a flush memory 106, and a non-volatile memory (NVRAM) 107, each one of them is connected to a bridge 108 via an internal bus 117 indigenous to the MPU 104. The MPU 104 executes all-round processes in the disk array system. The RAM 105 provides work space. The flush memory 106 stores codes and variables for operations. The NVRAM 107 stores after-mentioned error histories of every disk drive 103, threshold values of the total number of errors, the error rate, and its inclination. The bridge 108 is a bus protocol conversion circuit which provides an interface between an internal bus 117 and the data bus 115, such as a PCI (Peripheral Component Interconnect) standardized.” Further, see figures 1 and 3.).

Referring to claim 18, Sasamoto et al. disclose an array controller, wherein said array controller includes said demerit monitor (From line 24 of column 3, “The disk array control unit 101 includes a MPU 104, a RAM 105, a

flush memory 106, and a non-volatile memory (NVRAM) 107, each one of them is connected to a bridge 108 via an internal bus 117 indigenous to the MPU 104. The MPU 104 executes all-round processes in the disk array system. The RAM 105 provides work space. The flush memory 106 stores codes and variables for operations. The NVRAM 107 stores after-mentioned error histories of every disk drive 103, threshold values of the total number of errors, the error rate, and its inclination. The bridge 108 is a bus protocol conversion circuit which provides an interface between an internal bus 117 and the data bus 115, such as a PCI (Peripheral Component Interconnect) standardized." Further, see figures 1 and 3.).

Referring to claim 19, Sasamoto et al. disclose a storage controller coupled to a plurality of storage devices; wherein said demerit monitor is provided in the storage controller and is coupled to each of the plurality of storage devices for detecting data integrity errors in each of the plurality of storage devices, counting each data integrity error for each of the plurality of storage devices in a count (From line 24 of column 3, "The disk array control unit 101 includes a MPU 104, a RAM 105, a flush memory 106, and a non-volatile memory (NVRAM) 107, each one of them is connected to a bridge 108 via an internal bus 117 indigenous to the MPU 104. The MPU 104 executes all-round processes in the disk array system. The RAM 105 provides work space. The flush memory 106 stores codes and variables for operations. The NVRAM 107 stores after-mentioned error histories of every disk drive 103, threshold values of the total number of errors, the error rate, and its inclination. The bridge 108 is a

bus protocol conversion circuit which provides an interface between an internal bus 117 and the data bus 115, such as a PCI (Peripheral Component Interconnect) standardized." Further, see figures 1 and 3.), and when the count for one of the plurality of storage devices reaches a threshold limit, placing the one storage device into a forced failure state (From line 36 of column 5, "The calculating means 302 calculates an error rate and its inclination value from the total number of errors and the total access size of the disk drive in a way described later in FIG. 6 (see step S10). The judging means 303 judges if the disk drive is in need of disk changes from the total number of errors, the error rate, and the error rate inclination. When none of the calculated values exceeds the threshold value specified in the system, the disk array control unit 101 waits for further Read/Write requests from the host computer 100. If at least one of the calculated values exceeds the threshold value (however there may be some other combinations of the them, see step S11). The executing means 304 regards the disk drive as half-failed (see step 12). The reproducing means 307 copies or regenerates the data on the half-failed disk drive (see step S13), and stores the reproduced data on the spare disk drive 103c (see step S14). Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18). Then the disk array control unit 101 waits for further Read/Write requests from

the host computer 100.").

Referring to claim 20, Sasamoto et al. disclose a count table maintaining the count for each of the plurality of storage devices (From line 24 of column 3, "The disk array control unit 101 includes a MPU 104, a RAM 105, a flush memory 106, and a non-volatile memory (NVRAM) 107, each one of them is connected to a bridge 108 via an internal bus 117 indigenous to the MPU 104. The MPU 104 executes all-round processes in the disk array system. The RAM 105 provides work space. The flush memory 106 stores codes and variables for operations. The NVRAM 107 stores after-mentioned error histories of every disk drive 103, threshold values of the total number of errors, the error rate, and its inclination. The bridge 108 is a bus protocol conversion circuit which provides an interface between an internal bus 117 and the data bus 115, such as a PCI (Peripheral Component Interconnect) standardized.").

Referring to claim 22, Sasamoto et al. disclose said demerit monitor reconstructs data stored on the storage device in a restoration storage device and reformats the storage device (From line 48 of column 5, "The reproducing means 307 copies or regenerates the data on the half-failed disk drive (see step S13), and stores the reproduced data on the spare disk drive 103c (see step S14). Furthermore, the executing means 304 (1) disconnects the half-failed disk drive 103a from the disk array system (see step S15), (2) formats the data structure of the half-failed disk drive 103a (see step S16) and names the half-failed disk drive 103a as a new spare disk drive (see step S17), or (3) names the

half-failed disk drive 103a as a copy disk drive of the spare disk drive 103c (see step S18).").

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 9-12, 14, 25-28, 30, 39-42, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6442711 to Sasamoto et al. as applied to claims 1, 15, and 31 above, and further in view of US 4532628 to Matthews. Referring to claims 9, 25, and 39, although Sasamoto et al. do not specifically disclose said detecting data integrity errors in the storage device comprises: retrieving data from the storage device; comparing the retrieved data to redundancy data; and indicating a data integrity error if the retrieved data does not correspond with the redundancy data, detecting data defects by comparing to redundancy data is well known in the art. An example of this is shown by Matthews, from line 8 of column 3, "Data read from the memory 10 passes through a conventional data checker and correction unit 12. In the event that the unit 12 detects that the data read from the memory 10 is in error, the unit 12 corrects the data and restores the corrected data over the line 14 to the location read from memory 10." A person of ordinary skill in the art at the time of the invention would have been motivated to detect erroneous data because, specifically, from line 3 of column 2 of a Matthews, it is desirable to "[correct] "soft" failures before they become "hard" or double failures which may not be detectable while only minimally interfering with normal system operation", and

further, generally, one would want to work with correct data. Further, from line 34 of column 3 of Matthews, "In addition, the system causes an error indication to be stored in an error log in a conventional manner to identify the location at which the error was detected. The error indication in the error log can thereafter be reviewed and corrective maintenance performed, if deemed necessary." and from the title of Sasamoto et al. "System and method for avoiding storage failures in a storage array system", both Sasamoto et al. and Matthews are directed to corrective maintenance.

Referring to claims 10, 26, and 40, although Sasamoto et al. and Matthews do not specifically disclose said redundancy data is checksum data, using checksum data for error detection is notoriously well known in the art. Examiner takes official notice for checksums. A person of ordinary skill in the art at the time of the invention would have been motivated to use checksums because, from line 20 of column 3, "The exact technique used by the data check and correct circuit 12 for detecting and correcting errors in the data from the memory 10 is not critical to the present invention. Indeed, the prior art includes numerous methods and apparatus for detecting and correcting errors detected in digital computer systems and the like."

Referring to claims 11, 27, and 41, Sasamoto et al. disclose said retrieving data from the storage device is performed on a predetermined read schedule (From line 41 of column 3 (with emphasis), "The system according to the present invention includes circuitry to first determine the locations present in the attached dynamic semiconductor memory and then to **periodically** access, at a slow rate,

each present memory location.").

Referring to claims 12, 28, and 42, Sasamoto et al. disclose said retrieving data from the storage device comprises retrieving all of the data stored on the storage device; and said comparing the retrieved data to redundancy data comprises comparing all of the data stored on the storage device to redundancy data (From line 41 of column 3 (with emphasis), "The system according to the present invention includes circuitry to first determine the locations present in the attached dynamic semiconductor memory and then to periodically access, at a slow rate, each present memory location. As each memory location is read, the memory data checker and corrector 12 then checks and corrects any accessed location where a correctable error is detected. The failing location is listed in the error log. By periodically accessing each location in memory, soft errors can be detected and corrected before they become double or uncorrectable." Further, from the title, "System for periodically reading all memory locations to detect errors".).

Referring to claims 14, 30, and 44, although Sasamoto et al. and Matthews do not specifically disclose storing the count on the storage device, storing error data with the device the error data pertains to is notoriously well known in the art. Examiner takes official notice for storing error data on the storage device. An example of this is an error mapping table. A person of ordinary skill in the art at the time of the invention would have been motivated to store error data local to the device because it provides one to one correspondence and it localizes and compartmentalizes pertinent data.

Allowable Subject Matter

5. Claims 7, 8, 23, 24, 37, and 38 are allowed.

6. Claims 13, 29, and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Referring to claims 13, 29 and 43, the prior art does not teach or fairly suggest, in light of the parent respective claims, tracking the time elapsed after a first data integrity error; and decreasing the count if the time elapsed after the first data integrity error and before a second data integrity error is greater than a preset refresh period.

Response to Arguments

7. Applicant's arguments filed 9 July 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument that Sasamoto et al. do not teach or suggest "setting the count to a base level", Examiner has cited from the abstract, "The control unit includes means for storing a history of self recovered errors of each one of the plurality of data storage devices, means for calculating an error rate of each of the plurality of data storage devices on the basis of the history of errors, means for judging a necessity to execute a preventive maintenance of each one of the plurality of data storage devices from the error rate, and means for executing the preventive maintenance." From this passage, it is disclosed that an error rate is arrived at for determining, among other things, a necessity to execute a preventive maintenance of each one of the plurality of data storage devices. This error rate is not expressed as a total

number (which would not take into account a "rate"), but a count of the total number of errors *since* a previous error rate or predetermined interval. This can be more clearly seen as illustrated in figures 6(a)-6(c) and the corresponding passages in columns 5 and 6. Therefore, if an error rate is determined, there must be a base from which to measure subsequent counts, therefore, a base count level is set.

8. Applicant's arguments filed 9 July 2004, with respect to claims 13, 29, and 43 have been fully considered and are persuasive. The rejection of claims 13, 29, and 43 has been withdrawn.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is

(703) 308-7298, and after approximately October 15, 2004 will be (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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